QD-1000

Full Featured Single Chip Programmable IDDQ Monitor in SO-16

FEATURES

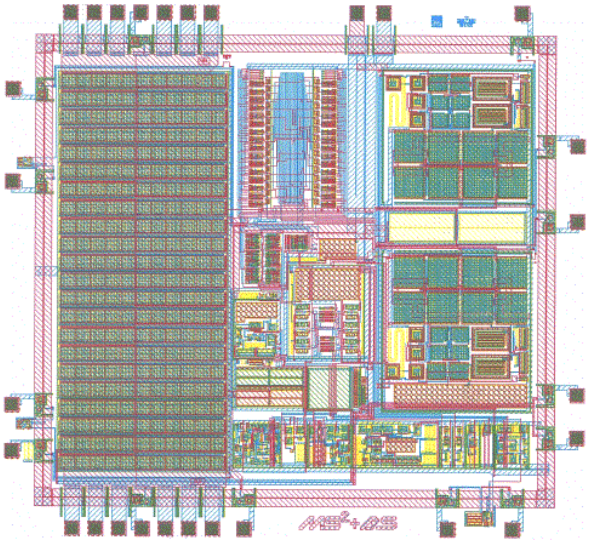
- 16-Pin SO Package
- Wide DUT Supply range: V_{DUT} = 0.5V to 7V
- Wide measurement range: I_{DDQ} = 0 – 1.5mA
- Maximum measurement rate: 30kHz
- High capacitive driving capability: up to 10µF
- High resolution: 1.5 nA_{RMS}
- 2-Wire Serial Programming Interface
- Low Power: I_{CC} Typ = 3mA with 12V Supply

APPLICATIONS

- ATE Load Board Applications
- High Speed IDDQ Measurements
- IDDQ Pass/Fail Measurements
- IDDQ Comparative Measurements

DESCRIPTION

The QD-1000 is a full featured, single chip, programmable quiescent supply current (I_{DDQ}) monitor, designed for loadboard applications. The QD-1000 operates according to the Stabilised Voltage Drop principle. It is designed to be inserted between the Automated Test Equipment (ATE) device power supply and the supply pin(s) of the Device Under Test (DUT), without the need to remove the decoupling capacitors. Its unique design ensures its transparency to both the ATE and DUT. It can drive high capacitive loads (up to several µF) and causes no additional voltage drop during the measurement.



QD-1000 Die

The QD-1000 offers the capability to perform accurate (up to 1.5nA_{RMS}) and repeatable high speed (up to 30kHz) quiescent supply current measurements. It has a wide measurement range (0-1mA). The QD-1000 requires a single positive supply, and provides, under all conditions, a stable, guaranteed and user programmable supply level to the DUT (0.5V to 7V).

The QD-1000 has an on-board compensated bypass switch, which minimises charge transfers. Its switch is capable of transferring large transient currents. To assure DUT supply stability, the bypass switch is automatically activated when the measured current is out of the monitor's measurement range. The QD-1000 can be configured for optimal performance in function of desired measurement speed/resolution and actual loading condition using a simple programming scheme. The monitor can be used in various application configurations.

The space-saving 16-pin CSOIC package and its operation with no external components provide the smallest IDDQ measurement solution available.

L.Bauwensstraat 20, B-8200 Brugge, Belgium, Tel.: +32 50 319273, Fax: +32 50 312350, http://www.QStar.be

ELECTRICAL SPECIFICATIONS

V_{CC} = +12.0V ±100mV, V_{DUT} = +5.000V ±1mV, T = +25°C

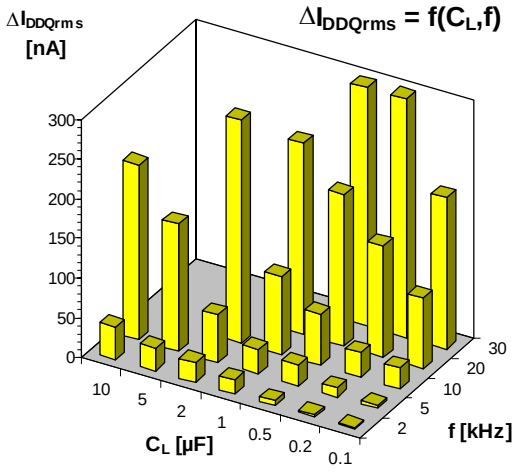
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Power Supply					
V_{CC}	Positive Supply Voltage	+12	+15	+18	V
I_{CC}	Supply Current			+3.5	mA
	Power consumption		36		mW
Measurement Characteristics					
I_{DDQ}	Measurement Range		0 – 1	0 – 1.5	mA
V_{DUT}	DUT Supply Voltage	0.5	3 – 5	7	V
	Resolution(1)	1.5		370.0	nA_{RMS}
	Measurement Rate	(2)	10	30	kHz
C_L	Loading Capacitance @ 10kHz	0.01		10	µF
	Linearity error @ I_{DUT} = 0.5mA			0.25	%
	Linearity error @ I_{DUT} = 1mA			0.5	%
	Measurement Offset		0.5	2.5	µA
ICVR	Internal Current to Voltage Ratio	4	5	6	mV/µA
RVCR	Reference Voltage to Current Ratio using Internal R_{PF}	250	200	167	nA/mV
Bypass Characteristics					
I_{DDT}	Transient Current			3	A
R_{ON}	On Resistance		300		mΩ
	Bypass Switch On Time			2.0	µs
	Bypass Switch Off Time			8.5	µs
Digital I/O					
V_{IH}	Digital Input High Voltage	2.4			V
V_{IL}	Digital Input Low Voltage			0.8	V
V_{OH}	Digital Output High Voltage	4.5		V_{CC}	V
V_{OL}	Digital Output Low Voltage			0.8	V
V_{PL}	Digital Pass Level	(3)(4)			V
V_{FL}	Digital Fail Level			0.8	V
I_O	Output Current	-10			mA
C_{IN}	Digital Input Capacitance			10	pF
Switching					
f_{CLK}	Maximum Clock Frequency			1	MHz
t_{CLK}	Minimum Clock Period	1			µs
t_1	MD Valid to CLK Setup	200			ns
t_2	MD Valid to CLK Hold	200			ns

NOTES

(1) Configuration dependant
(2) The QD-1000 can be used to perform static measurements
(3) Pass level is settable via pull-up resistor, PF output is open drain
(4) During bypass mode the PF output is not valid.

ACCURACY & RESOLUTION

The accuracy and measurement resolution of the QD-1000 is function of the desired measurement speed, the capacitive loading condition and the selected operational configuration. Alternatively in function of the actual loading condition and the desired resolution the measurement speed and the programming configuration can be selected. The figure below gives an overview of the measurement resolution in function of loading condition and measurement speed.



ΔIDDQrms = f(CL,fTest) [nA]					
fTest / CL	2 kHz	5 kHz	10 kHz	20 kHz	30 kHz
0.1 µF	1.5	4	26	89	190
0.2 µF	3	12	31	140	330
0.5 µF	6	26	65	190	370
1.0 µF	18	31	98	240	
2.0 µF	25	60	280		
5.0 µF	29	160			
10.0 µF	41	220			

ABSOLUTE MAXIMUM RATINGS

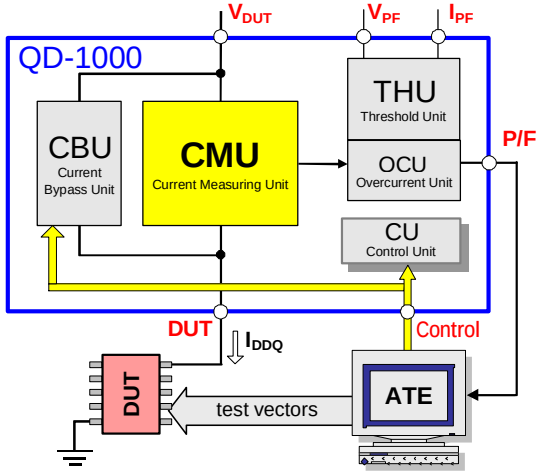
Parameter	With Respect To	Min	Max	Units
V_{CC}	GNDA	-0.5	+18	V
V_{CC}	GNDD	-0.5	+18	V
Digital Inputs	GNDD	-0.5	V_{CC} + 0.5	V
Digital Output	GNDD	-0.5	V_{CC}	V
Digital Output	GNDD	-10	0	mA
VPF	GNDA	-0.5	V_{CC} + 0.5	V
VDUT	GNDA	-0.5	V_{CC} + 0.5	V
IPF	GNDA	-1.5	0	mA
I_{DDT} (1)	GNDA	-3	3	A
Operating Temperature Range		-55	+125	°C
Storage Temperature		-65	+150	°C
Lead Temperature (10sec) (2)			+300	°C

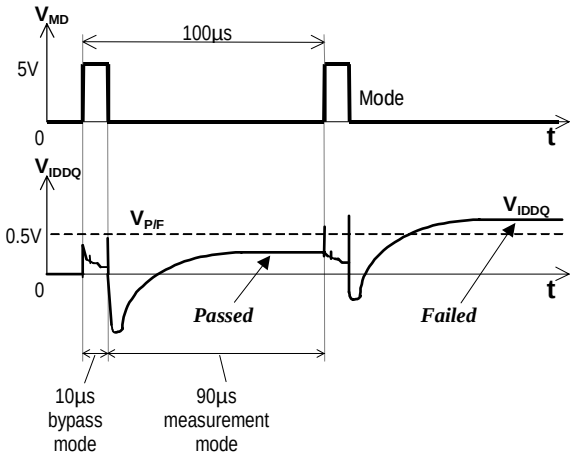
(1) Duration of the current pulse 1ms max, duty ratio 1% max.
(2) Manual soldering is recommended using SnPB solder

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING MODES

The QD-1000 has two main operating modes, namely programming mode and normal operation mode. The programming of the QD-1000 is done under control of the MD and the CLK inputs. This is described in more detail in the next section. In normal operation mode an additional bypass mode and measurement mode can be distinguished. QD-1000 operates in normal mode when the CLK input is inactive. The selection between bypass and measurement mode is controlled by the MD input. When the MD input is "H" then the internal Bypass switch is closed and the monitor operates in bypass mode. When the MD input is "L" then the monitor operates in measurement mode and the quiescent current is measured. When the measured current is out of the monitor's measurement range, the QD-1000 switches automatically back to bypass mode. To control the QD-1000, standard TTL levels should be used. The figures below show a functional block diagram as well as a typical measurement cycle (normal mode operation, CLK = "L", 10 kHz operation).

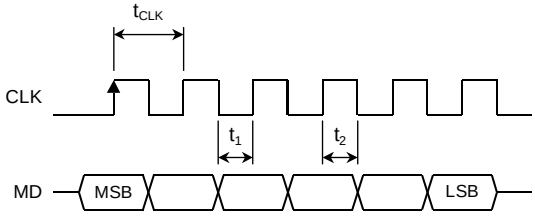




CONFIGURING THE QD-1000

To select the optimal QD-1000 operation configuration in function of resolution, speed and loading conditions, the QD-1000 can be programmed. A simple 2-wire programming scheme is used to load the internal shift register with the appropriate code.

The QD-1000 has an on-board 6 bits configuration register. This allows entering a configuration code in the range from 00h to 3Fh. The 2 most significant bits define the characteristic of the embedded filters and determine the measurement rate. The remaining four bits determine the damping factor of the regulating loop of the CMU to be selected in function of the loading capacitance. Typical configuration values in function of loading conditions and measurement speed are given in the table below. More information on configuring the QD-1000 can be found in application note AN0002.



f_{Test} / C_L	2 kHz	10 kHz	30 kHz
0.1 µF	3F	1E	07
0.5 µF	3E	18	03
2.0 µF	37	13	
5.0 µF	34	23	
10.0 µF	33	13	
All codes are listed in hexadecimal format			

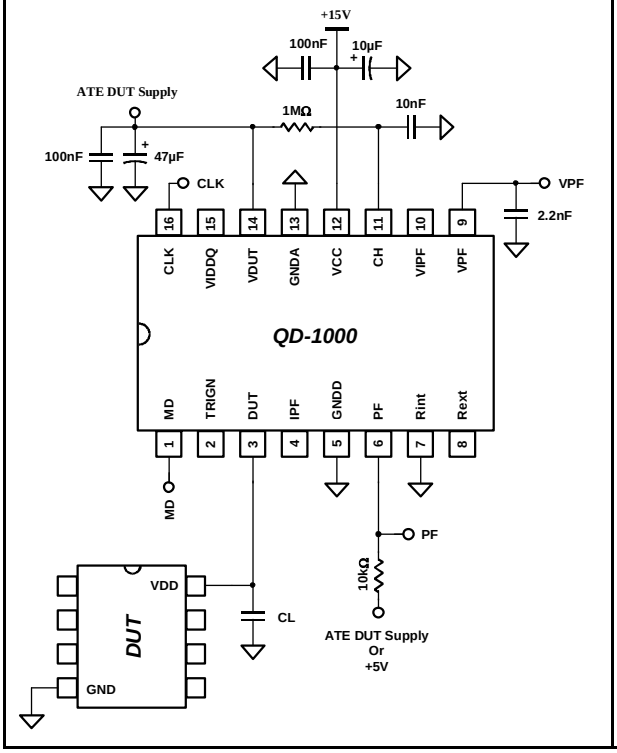
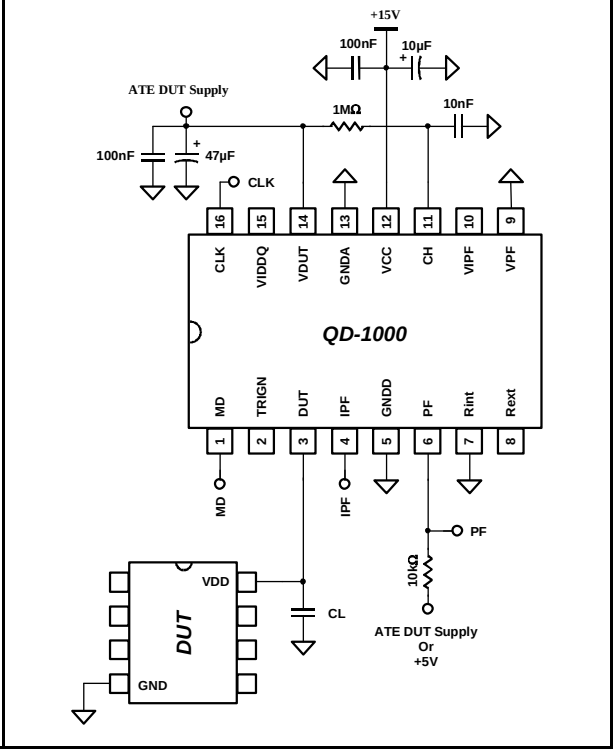
The configuration is loaded by applying a series of 6 pulses to the CLK input and the corresponding data should be provided on the MD input as shown in the figure below. The maximum clock frequency is 1MHz. The data is stored on the rising edge of the CLK input clock. The data must be entered with the MSB first.

NOTES:

1. To assure that the monitor always starts operating from a well known state, an internal power on reset circuit clears the configuration register during power-up, hence the content of the configuration register at start up is 00h, being the default configuration. As a result the QD-1000 needs to be reconfigured each time after a power-down, power-up cycle.
2. Although not directly advised, the QD-1000 can also be used without configuring, by using the default configuration. The default configuration allows as such the fastest possible measurement, but depending on the actual application and the high AC gain of the regulation loop, a damped oscillation may occur on the measurement signal (but not affecting the DUT output) when the QD-1000 switches from Bypass state to Measurement state. This may prolong the actual measurement period needed for performing accurate measurements. To avoid these potential oscillations the minimal configuration to be used is 03h. More information on the programming of the QD-1000 can be found in application note AN0002.
3. The values specified in the table above are recommended values. Optimal values may differ due to application constraints. More information on configuring the QD-1000 can be found in application note AN0002.

TYPICAL APPLICATIONS

The QD-1000 provides the possibility to set the pass/fail level either by using a reference current sink or reference voltage source. Internally the QD-1000 compares the DUT current with a reference current. To allow the pass/fail level to be set by voltage, the QD-1000 contains a built-in 5kΩ resistor, as part of the on-board V/I converter. The diagrams below show the application diagram when using a reference current sink (IPF) or when using a reference voltage source (VPF). It is recommended to use the plug and play interface boards QI-0002 & QI-0003. The QI-0002 & QI-0003 are dedicated QD-1000 interface boards that contain the QD-1000 as well as all the necessary component needed for the proper operation of the QD-1000, hereby simplifying the load board design and turning the QD-1000 into a plug and play application.

PASS/FAIL LEVEL SET BY REFERENCE VOLTAGE	PASS/FAIL LEVEL SET BY REFERENCE CURRENT
	

Note that a calibration of the V/I converter is needed for proper operation. Since the V/I characteristic of the V/I converter is linear, a simple 2-point measurement is sufficient to perform the calibration. More information on how to calibrate the QD-1000 can be found in application note AN0006.

To avoid the calibration of the V/I converter, the QD-1000 supports the use of an external accurate resistor (R_{ext}) instead of using the internal 5kΩ resistor (R_{int}). More information on using an external V/I converter can be found in application note AN0003.

There are no special requirements concerning the PCB layout. Note that the length of routes connecting the hold capacitor to the *CH* pin should be kept to a minimum. The decoupling capacitors on the monitor supply (VDD) should be placed as close as possible to the QD-1000 pins. The P/F output track should lead rather far from other sensitive analog tracks, because this comparator output can cause interference during switching.

PACKAGE & PIN DESCRIPTION

The QD-1000 is packed in a 16 pins CSOIC (Ceramic Small Outline Integrated Circuit) package for surface mount applications.

Pin #	Name	Type	Function
1	MD	I	Mode control ("H" = Bypass, "L" = Measurement) – Data input
2	TRIGN	O	External bypass control
3	DUT	O	DUT supply pin
4	IPF (1)	O	Current reference to set the Pas/Fail level
5	GNDD (2)	S	Monitor digital ground
6	PF (3)(4)	O	Pass/Fail flag ("H" = pass – measured current below threshold, "L" = fail – measured current above threshold)
7	Rint	C	Sense resistor control pin. This pin must be grounded if the internal V/I converter is used and must be left floating if an external V/I converter is used.
8	Rext	C	Control pin to connect an external resistor that serves as a V/I converter. This pin must be left floating if the internal 5kΩ resistor is used.
9	VPF (1)	I	Voltage reference input to set the Pass/Fail level
10	VIPF (5)	O	Analog output of the Current Reference Unit
11	CH	I	Connection for external hold capacitor
12	VCC	S	Monitor supply voltage
13	GNDA (2)	S	Monitor analog ground
14	VDUT (6)	I	DUT supply reference input
15	VIDDQ (5)	O	Analog output of the Current Measurement Unit
16	CLK	I	Clock input

(1) Pins 4 & 9 are to be used exclusively, VPF must be grounded when not used by connecting a shunt on JP1, IPF must be left floating when not used.

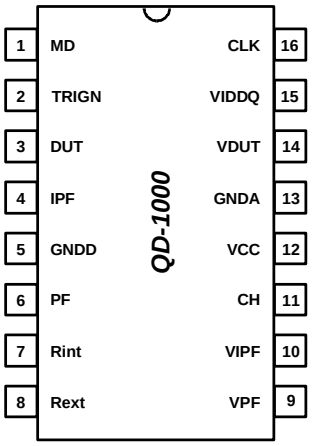
(2) For optimal performance of the QD-1010HC monitor, the AGND pin and the GND pin must be connected to the same ground level as the DUT supply being monitored. Preferably these pins are connected using a ground plane.

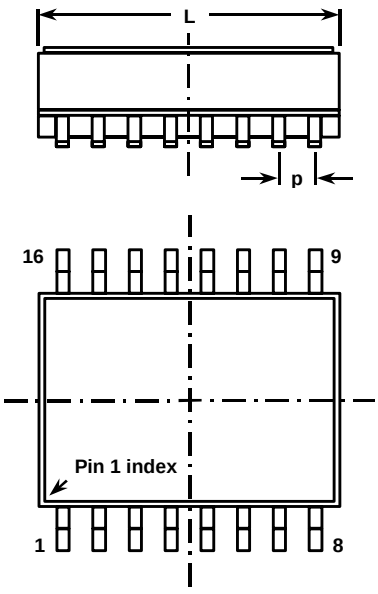
(3) The PF output is an open drain ouput. Note that an appropriate protection resistor R_S must be chosen as the amount of current the open drain output can sink is limited to 10mA. Typical values for R_S i.f.o. voltage level are: 100Ω @ 3.3V; 330Ω @ 5.0V; 500Ω @ 7.0V.

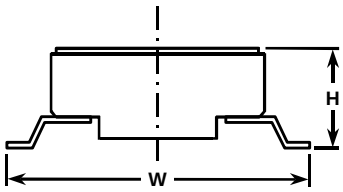
(4) During bypass mode the PF output is not valid.

(5) Sensing the VIDDQ and VIPF outputs should be done with care as the VIDDQ and VIPF output has no real driving capability. It is advised to connect a buffer circuit to this output when sensed.

(6) The VDUT pin must be permanently connected to a voltage source and must not be left floating..







Unit	L	W	H	p
mm	10.5	10	2.15	1.27
inches	0.41	0.39	0.085	0.050

LIST OF APPLICATION NOTES

A series of applications notes concerning the QD-1000 are listed below:

AN0001	Performing measurements with the QD-1000
AN0002	Configuring options for the QD-1000
AN0003	Using the QD-1000 for measuring small currents with enhanced resolution
AN0004	Using the QD-1000 to perform comparative measurements
AN0005	Improving the bypass switch characteristics of the QD-1000
AN0006	Calibrating the QD-1000